Digital Logic: From Gates to Functions and Memory

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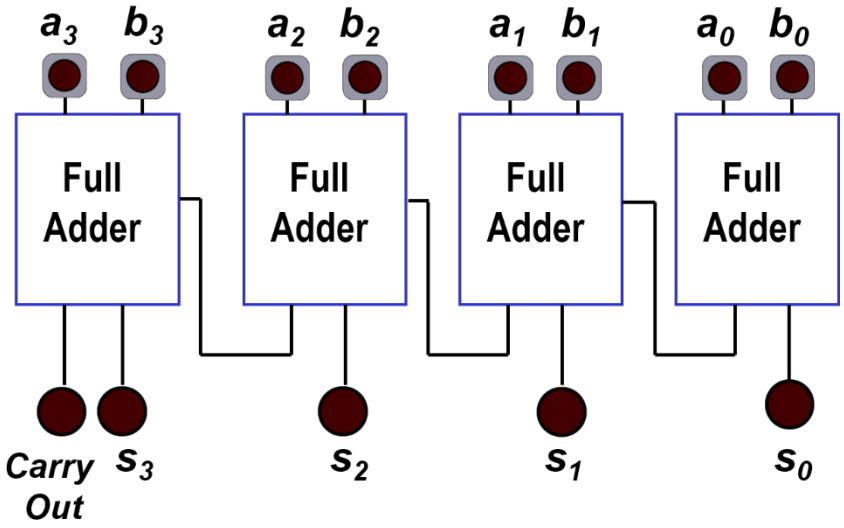
Exercise: Build a 5-bit Adder

The diagram shows a 4-bit adder. Extend the design to build a **5-bit adder.** Space your adder chips about one gate-width apart so that you have room to work.



Test these values and a few others. With eight inputs, there are $2^8 = 256$ possible input combinations. Testing them all in class is not a good use of time.

A_4	B_4	A_3	B_3	A_2	B_2	A_1	B_1	A_0	B_0	S_3	S_2	S_1	S_0	C_O
0	0	0	0	0	0	0	0	0	0					
0	1	0	1	0	1	0	1	0	1					
		0	0	0	0	0	0	1	0					
0	0	1	1	1	1	1	1	1	1					

Exercise:

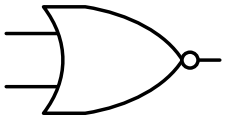
If a particular full adder requires one nanosecond to complete its computation, how long will a 32-bit ripple-carry adder take to complete an addition? A 64-bit ripple-carry adder?

Another Gate

The NOR gate looks like a NOT gate with a circle at the output. The circle is called a negation bubble. NOR is an abbreviation for NOT-OR. Compare the truth table to that of the OR gate.

NOR gate

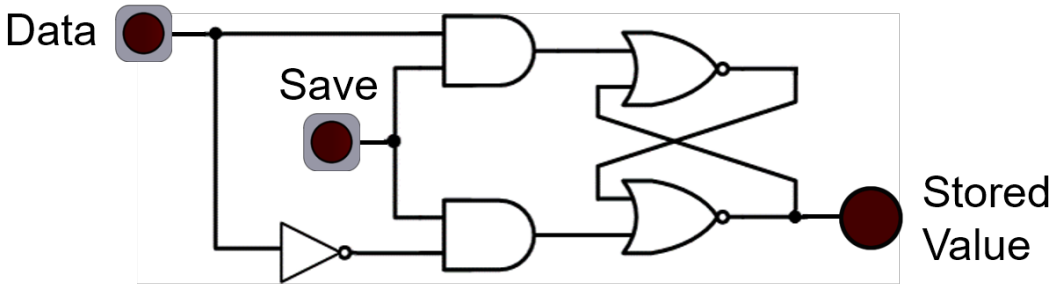
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0



Exercise:

Build a clocked D-Latch. Use pushbuttons for the inputs marked "Data" and "Save."

When you have your D-latch working, delete the pushbutton marked "Save" and replace it with the Digital Works clock generator. It's in the parts bar, just to the left of the pushbutton, and looks like this: 



If we were building an actual computer, the computational circuits, like the adder, would have to finish their work within the time of each clock cycle. To make the clock faster, all the other circuits must also be made faster, or we would risk storing data before the computations were complete.

Note: The D-latch is transistor memory. Computer designers use transistor memory when speed is needed. The RAM in generally dynamic RAM, or DRAM. It uses charge storage to store bits. It's somewhat slower, but much less expensive than transistor memory.